WHAT IS CLAIMED IS:

1. An active driver, comprising:

an internal voltage-generating unit for converting an external power supply voltage into an internal voltage according to a reference voltage and outputting; and

at least one internal voltage drop control unit that is operated by an enable signal generated by detecting a voltage level of the internal voltage, for stabilizing the internal voltage to a constant voltage level.

2. The active driver as claimed in claim 1, wherein the internal voltage drop control unit comprises:

a switching unit operated by the enable signal; and

a sub driver operated by a signal to control the operation of an output driver of the internal voltage-generating unit, for transferring the power supply voltage transferred through the switching unit.

3. The active driver as claimed in claim 2, wherein the sub driver is a PMOS transistor.

4. The active driver as claimed in claim 1, wherein the internal voltage-generating unit is controlled so that the unit is operated according to an active signal that is generated in an active operation.

5. The active driver as claimed in claim 1, wherein the means for generating the enable signal comprises:

a detection unit for detecting the internal voltage according to the reference voltage;

a voltage booster unit for boosting the output of the detection unit; and

an output unit for outputting the enable signal depending on the output of the voltage booster unit.

6. The active driver as claimed in claim 5, wherein the detection unit is a current mirror that operates according to an active signal.

7. The active driver as claimed in claim 5, wherein the detection unit comprises:

a current mirror that operates according to an active signal; and

a stabilization unit for stabilizing the output of the current mirror and outputting.

8. The active driver as claimed in claim 5, wherein the voltage booster unit is a level shifter.

9. The active driver as claimed in claim 5, wherein the output unit comprises:

a PMOS transistor serially connected between a power supply voltage source and a node and operated according to a power-up signal;

a first NMOS transistor connected between the node and a ground voltage source, wherein the first NMOS transistor is turned on by the output of the voltage booster unit ;

a second NMOS transistor serially connected between the first NMOS transistor and the ground voltage source, wherein the second NMOS transistor is turned on by a delay signal of the active signal;

a latch unit for latching the potential of the node and outputting; and

a NAND gate for performing a NAND operating for an output signal of the latch unit, the active signal and the delay signal.